AMENDMENTS TO THE CLAIMS

1. (Currently amended) An electronic memory device, comprising:

at least one memory cell;

a write circuit defining an output node, and selectably connecting the at least one memory cell to the output node to permit a discharge associated with a write operation to flow to the output node; ~~and~~

a write strength selection circuit that modifies at least one characteristic of the discharge flowing to the output node, wherein the write strength selector circuit has a strong write state associated with a first value of the at least one characteristic, and a weak write state associated with a second value of the at least one characteristic.

2. (Canceled)

3. (Original) The device of claim 1, wherein the write strength selection circuit has a selectable first impedance and a selectable second impedance greater than the first impedance, wherein the first impedance is associated with a strong write operation and a second impedance is associated with a weak write operation.

4. (Original) The device of claim 1, wherein the at least one characteristic is at least one of a current level and a quantity of charge.

5. (Currently amended) The device of claim 1, wherein the write strength selection circuit comprises a first transistor, to provide a strong write operation, and a second transistor, to provide ~~the~~ a weak write operation.

6. (Original) The device of claim 1, wherein the write strength selection circuit comprises a plurality of circuit elements electrically connected in parallel to the output of the write

circuit, the plurality of circuit elements selectable in a plurality of combinations to provide a plurality of weak write operations and at least one strong write operation.

7. (Original) The device of claim 6, wherein the plurality of circuit elements comprise a plurality of transistors each having a different gate parameter.

8. (Original) The device of claim 1, wherein the at least one memory cell comprises a plurality of memory cells arranged in a plurality of rows and a plurality of columns, and further comprising a plurality of pass circuits associated with the plurality of columns, each of the plurality of pass circuits selectably connecting the associated column to the output node.

9. (Original) The device of claim 1, wherein the write circuit comprises at least one inverter.

10. (Original) The device of claim 1, wherein at least a portion of the discharge flowing to the output node flows through the output node.

11. (Original) The device of claim 1, wherein the at least one memory cell comprises a plurality of static random access memory cells.

12. (Original) The device of claim 1, wherein the write circuit comprises three inverters that selectably connect the at least one memory cell to the output node via one of a bit line and a complementary bit line.

13. (Original) The device of claim 1, further comprising an output node stabilization circuit in electrical communication with the output node to charge the output node to a preselected voltage level.

14. (Original) The device of claim 13, wherein the preselected voltage level is one of a write operation precharge voltage level, a ground voltage level, and a voltage level between the write operation precharge voltage level and the ground voltage level.

15. (Original) The device of claim 1, further comprising at least one failure-analysis memory cell that has an intentional defect.

16. (Original)A method for testing data retention of an electronic memory device comprising at least one memory cell, the method comprising:

providing a write circuit defining an output node, and selectably connecting the at least one memory cell to the output node to permit a discharge associated with a write operation to flow to the output node;

storing a value in the at least one memory cell;

directing a weak write operation to the at least one memory cell by controlling at least one characteristic of the discharge flowing to the output node; and

sensing the memory cell to determine if the stored value changed in response to the weak write operation.

17. (Original) The method of claim 16, wherein the memory device comprises an array of memory cells, and further comprising determining a strong write strength of the array by empirically determining an effective overwrite strength for the array of memory cells.

18. (Original) The method of claim 16, wherein directing a weak write operation comprises writing for a preselected period of time.

19. (Original) The method of claim 16, wherein controlling a current of the discharge comprises controlling an impedance of a circuit in electrical communication with the output node.

20. (Original) The method of claim 16, wherein the write strength circuit selectably provides a strong write strength and a plurality of weak write strengths, and further comprising writing to the memory cell with a greater one of the plurality of weak write strengths if the stored value has not changed.

21. (Original) A method for failure analysis of an electronic memory device comprising an array of memory cells, the method comprising:

determining which cells of the array are weak;

providing a write circuit defining an output node, and selectably connecting the at least one memory cell to the output node to permit a discharge associated with a write operation to flow to the output node;

storing a value in the at least one memory cell;

directing a weak write operation to the at least one memory cell by controlling at least one characteristic of the discharge flowing to the output node; and

sensing the at least one memory cell to determine if the stored value changed in response to the weak write operation; and

repeating the weak write operation, with a greater write strength, until the stored value changes to determine a failure mode of the at least one memory cell.

22. (Original) The method of claim 21, further including the step of providing in the electronic memory device intentional defects that are associated with manufacturing defects, and determining the weak write strengths associated with the intentional defects to permit the determination of the failure mode of the at least one memory cell.